PRO-LOG
CORPORATION

STD 7000

7702A
16K BYTE-WIDE
MEMORY CARD

USER'S MANUAL

7/82

FOREWORD

This manual explains how to use Pro-Log's 7702A 16K Byte-Wide Memory Card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7702A. We welcome your suggestions on how we can improve our instructions.

The 7702A is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: *Microprocessor User's Guide* and the *Series 7000 STD BUS Technical Manual.* If you would like a copy of these documents, please submit your request on your company letterhead.

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SECTION 1
Purpose and Main Features

PURPOSE

The 7702A 16K Memory card is designed to be a flexible part of the memory in your STD system. Its eight sockets, designed for devices conforming to the JEDEC 28-pin dual inline standard pinout allow the use of 2K ROMs and RAMs.

The MEMEX line can be used to implement a maximum of memory with a minimum of hardware. A system using Pro-Log's 7804 Z80A processor card and multiple 7702A cards can have up to 128K of memory with no additional signal lines.

The 7702A can also respond to an external Segment Select line, allowing it to participate in large-scale bank select schemes. The Segment Select line can be controlled by a memory segment controller or I/O ports. Also, the 7702A can be tailored to fit small scale applications. Unused sockets may be disabled, allowing the card to occupy as little as 2K bytes of memory space.

The 7702A has 3 jumper selectable combinations of memory parts. These combinations are 16K of ROM; 8K of ROM and 8K of RAM; or 16K of RAM.

FEATURES

- Eight 2K Memory Sockets — 16 Kilobyte Capacity
- Either 16K of ROM, 16K of static RAM, or 8K of each
- User-selectable card address range
- Provision for Memory segmentation
- Responds to MEMEX high or low
- Processor independent — use with 8085, Z80A, 6800, 6809, 8088, and others

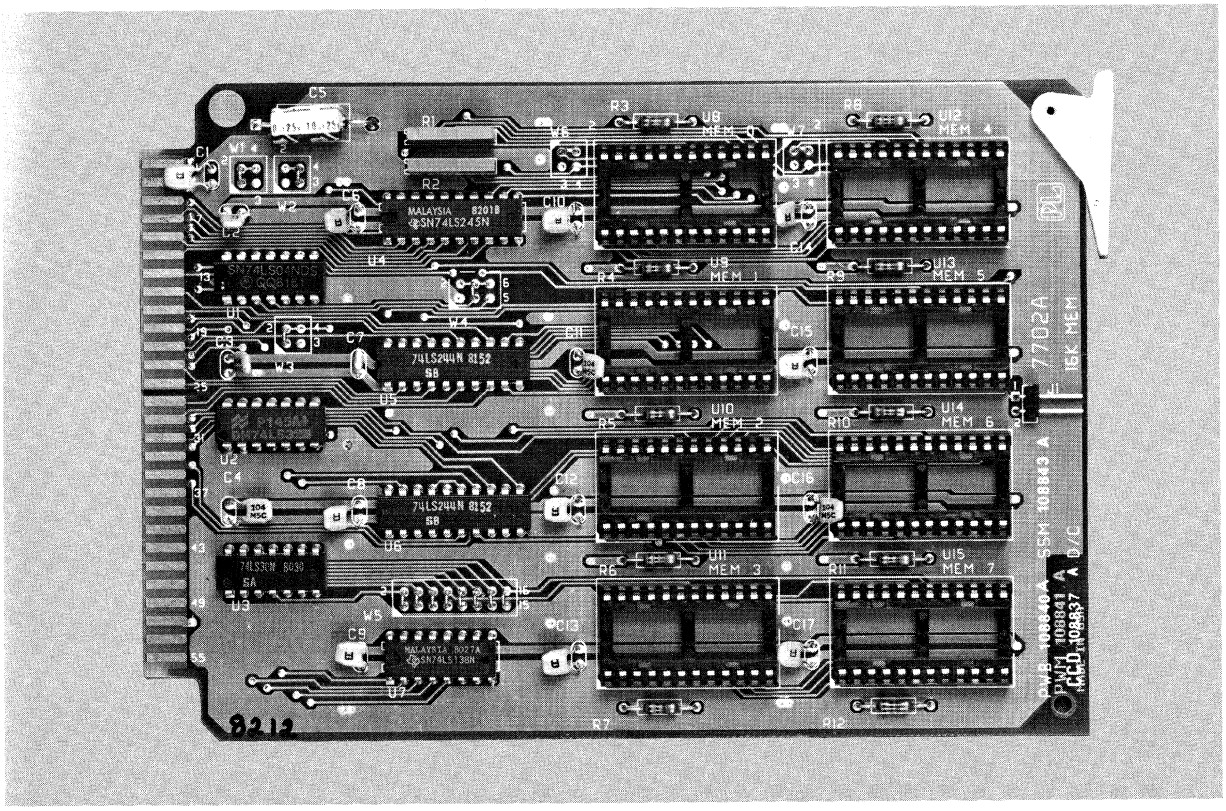


Figure 1-1. 7702A 16K Byte-Wide Memory Card.

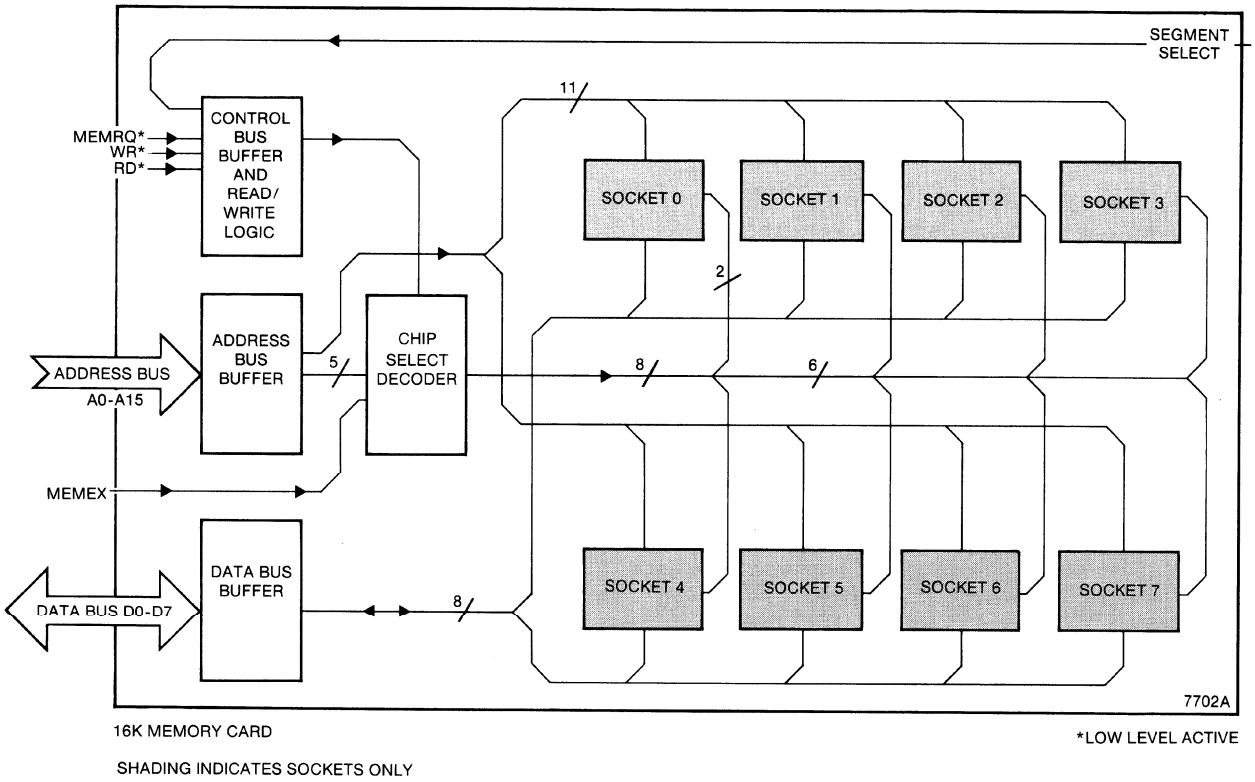


Figure 1-2. Block Diagram of 7705A 32K EPROM Memory Card.

SECTION 2
Installation and Specifications

INSTALLATION

The 7702A operates as part of an STD BUS card rack system. It can plug directly into the STD BUS backplane, as shown in Figure 2-1, or extend from the motherboard with a 7901 Extender Card. To use the 7901, plug it into any slot in the card rack, and plug the 7702A into the connector on the 7901. This makes the 7702A accessible for testing.

The 7702A can occupy any slot in the card cage. It should be installed with the card ejector towards the top of the card rack as shown in Figure 2-1.

If the external Segment Select line is used, it should be attached as shown in Figure 2-2. The connector type is a 2-pin 0.1-inch center connector. The cable should be a twisted pair, consisting of one signal line and one ground line for added noise immunity. The Pro-Log RC704 cable can be used for this purpose and can connect the 7702A to an I/O card such as Pro-Log's 7605.

CAUTION

To prevent possible damage to your STD BUS system, insure that power is off before inserting or removing a card from the card rack.

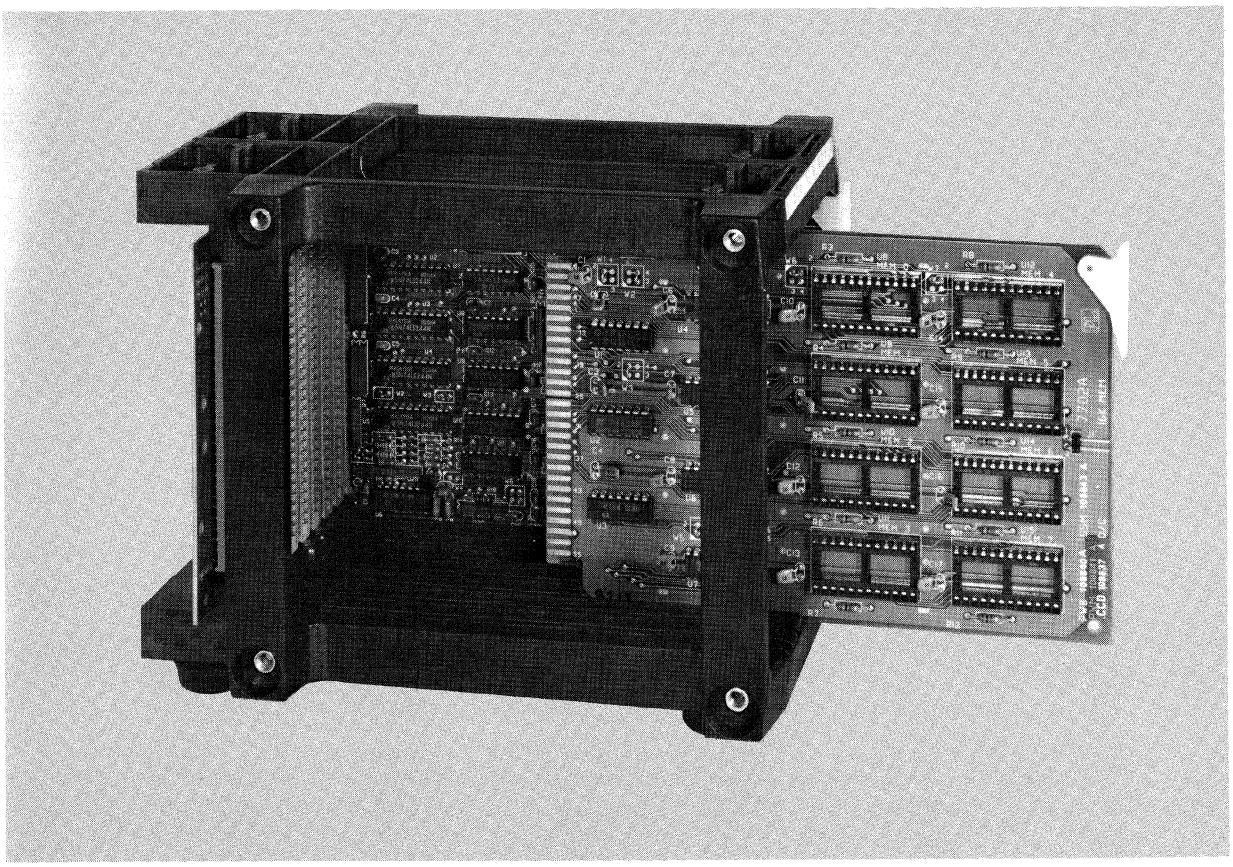


Figure 2-1. 7702A Installation

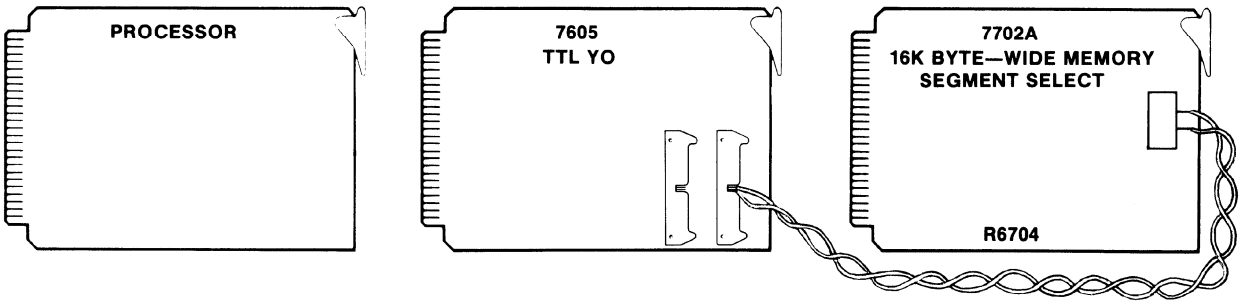


Figure 2-2. 7702A Segment Select Connector

WIRE JUMPERS

Some 7702A optional functions are selected by wire jumpers. When removing and replacing these jumpers, cut the jumper in half, then desolder and remove each half individually. Any remaining solder should be removed before new jumpers are installed. This procedure will prevent damage to circuit traces.

Most 7702A optional functions can be selected by permanent 0.025 in. square post headers which can be connected by slip-on, slip-off connectors. Part numbers for these connectors and headers are listed in Fig. 2-3. Figure 2-4 shows the location of these jumpers.

PART	MANUFACTURER PART NUMBER	
	ELCO CORP.	BERG ELECTRONICS
2-PIN HEADER	00 8261 02 32 00 852	65611-102
4-PIN HEADER	00 8261 04 32 00 852	65611-104
6-PIN HEADER	00 8261 06 32 00 852	65611-106
8-PIN HEADER	00 8261 08 32 00 852	65611-108
CONNECTOR	00 8261 02 42 00 870	

Figure 2-3. Part Numbers for 7702A Option Jumpers

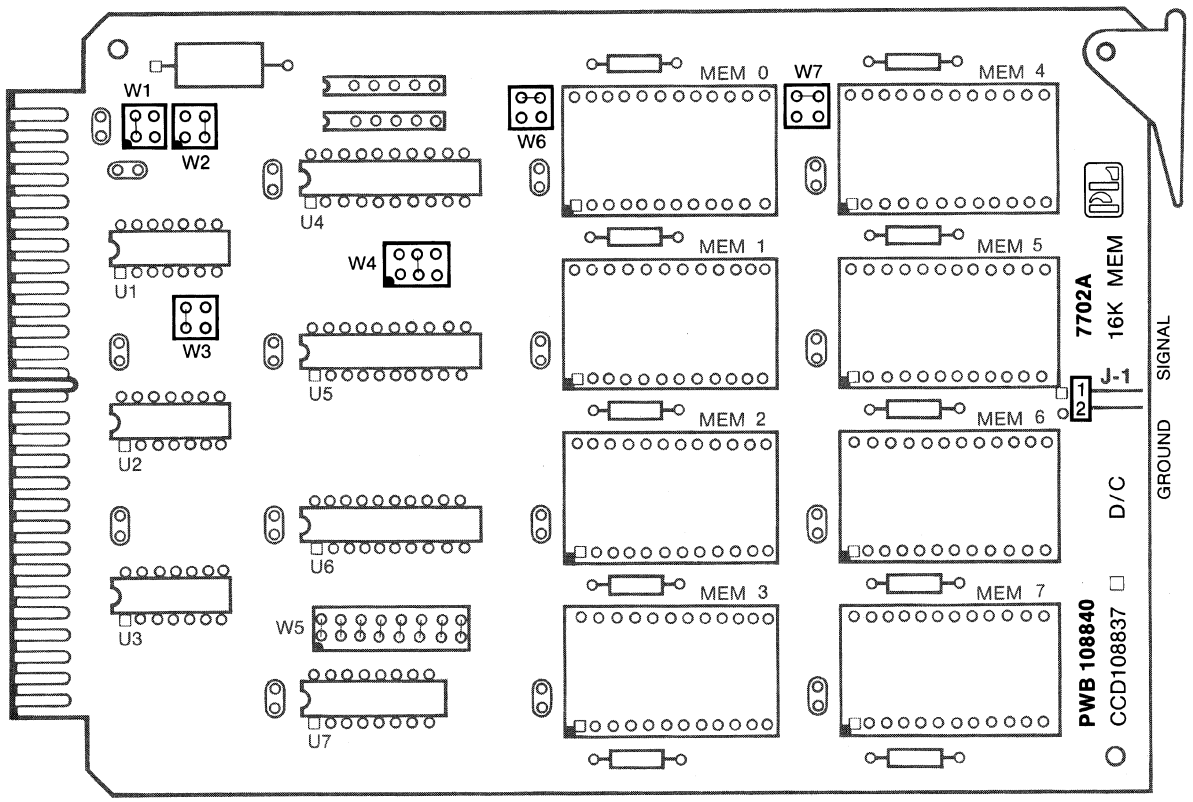


Figure 2-4. 7702A Physical Locations of Features.

MEMORY DECODER

The 7702A may be configured to operate within any of the four 16K-byte address ranges available within the addressable 64K memory space.

The specific 16K-byte address range is determined by the locations of jumpers W1 and W2 (see Fig. 2-4). To select the appropriate block using W1 and W2, see Fig. 2-5.

To determine the address range of each socket see Figure 2-6.

Address Range of Card	W1 Jumper Location	W2 Jumper Location
0000-3FFF	1,2	1,2
4000-7FFF*	1,2	3,4
8000-BFFF	3,4	1,2
C000-FFFF	3,4	3,4

*Address as shipped

Figure 2-5. 7702A Card Addressing Jumpers.

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Card Address Range
PAGE 0X	SOCKET 0								SOCKET 1								0000 TO 3FFF
1X	SOCKET 2								SOCKET 3								
2X	SOCKET 4								SOCKET 5								
3X	SOCKET 6								SOCKET 7								
PAGE 4X	SOCKET 0								SOCKET 1								4000 TO 7FFF
5X	SOCKET 2								SOCKET 3								
6X	SOCKET 4								SOCKET 5								
7X	SOCKET 6								SOCKET 7								
PAGE 8X	SOCKET 0								SOCKET 1								8000 TO BFFF
9X	SOCKET 2								SOCKET 3								
AX	SOCKET 4								SOCKET 5								
BX	SOCKET 6								SOCKET 7								
PAGE CX	SOCKET 0								SOCKET 1								C000 TO FFFF
DX	SOCKET 2								SOCKET 3								
EX	SOCKET 4								SOCKET 5								
FX	SOCKET 6								SOCKET 7								

Figure 2-6. 7702A Socket Address Ranges.

Any socket on the 7702A can be disabled. The memory space formerly occupied by the socket then becomes available for use by other cards in the system. To disable a socket, cut or remove the appropriate jumper. The location of the jumpers, jumpers W5, is shown in Figure 2-4. Figure 2-7 shows which jumper affects each socket.

Memory Socket	Memory Socket Disable Jumpers	Address Range as Shipped
0	W5- 1, 2	4000-47FF
1	W5- 3, 4	4800-4FFF
2	W5- 5, 6	5000-57FF
3	W5- 7, 8	5800-5FFF
4	W5- 9,10	6000-67FF
5	W5-11,12	6800-6FFF
6	W5-13,14	7000-77FF
7	W5-15,16	7800-7FFF

Figure 2-7. 7702A Memory Socket Disable Jumpers.

MEMORY TYPE

The 7702A uses two kinds of memory: 2K ROMs or RAMs. The eight memory sockets are designed to accept memory components compatible with the JEDEC 28-pin standard pinout. The sockets can only be configured for ROM or RAM in groups of four. The groups will consist either of sockets 0 thru 3, or sockets 4 thru 7.

After having chosen the memory mapping best suited to your needs, as discussed in the Memory Decoder section, the sockets should be configured for RAM or ROM operation.

This is done with Jumpers W6 and W7. Jumper W6 configures sockets 0 to 3 and jumper W7 configures Sockets 4 to 7.

As shipped, the 7702A is configured for all ROM operation. To configure the card for RAM see Figure 2-8.

Rom/Ram Select Jumpers	Type Devices	Sockets
W6-1,2	ROM	0-3
W7-1,2	ROM	4-7
W6-3,4	RAM	0-3
W7-3,4	RAM	4-7

Figure 2-8. 7702A ROM/RAM Configuration Jumpers.

Figure 2-9 is a list of pin-compatible memory components for use on the 7702A card. The memory components, which have been tested and are recommended, are indicated by an asterisk. If you wish to use other memory components, compare its data sheet to the socket configurations.

CHIP #	ORGANIZATION	ACCESS
INTEL CORPORATION		
21812	2K SRAM	150
*2716	2K EPROM	350-650
MOSTEK CORPORATION		
MK34000	2K ROM	350
*MK2716	2K EPROM	300
MK4082	2K SRAM	
NATIONAL SEMICONDUCTOR		
*MM2716	2K EPROM	350-450
MOTOROLA		
*MCM2716	2K EPROM	250-450
TEXAS INSTRUMENTS		
*TMS2516	2K EPROM	
MITSUBISHI		
*M58725	2K SRAM	200
NEC MICROCOMPUTERS		
*uPD2716	2K EPROM	450
AMERICAN MICROSYSTEMS (AMI)		
S4028	2K SRAM	200
SYNERTEK		
*SY2716	2K EPROM	350-450
OKI		
*MSM5128	2K SRAM	150-200-250
TOSHIBA		
*TMM2016	2K SRAM	150-250

*Recommended Devices

Figure 2-9. Memory Components List for 7702A.

MEMEX

The function and operation of the MEMEX line will be explained in Section 3. This section explains the jumper options affecting MEMEX.

MEMEX can be used to enable the 7702A card. Using this method, two 7702A's can occupy the same address field, only one of which is enabled at a time depending on the logic state of the MEMEX line.

As shipped, the 7702A card is enabled when MEMEX is low. To reverse this polarity, remove jumper 3-4 of W4 and replace it with one at position 5-6. The location of this jumper is shown in Figure 2-4. When two of these cards will occupy the same memory address space, one should have its polarity changed.

It is important to ensure that the MEMEX line is not left floating. The line must be either controlled by another card in the system, or tied to ground on the 7702A itself. Pro-Log processor cards either control the MEMEX line or simply tie it to ground. If there is no card in the system controlling MEMEX, or if the card is to disregard MEMEX, jumper W4 can be removed from position 3-4 and be replaced by one at position 1-2. This will tie the line to ground and permanently enable the card.

SEGMENT SELECT

The function and operation of the Segment Select line will be explained in Section 3. This section is to explain the jumper options affecting Segment Select.

The Segment Select line is not a part of the STD BUS. It is an external line which is accessible on the card ejector side of the 7702A. Figure 2-4 shows the location of the connector.

The connector type is a 2-pin, 0.1-inch center connector. The cable should be a twisted pair, consisting of one signal line and one ground line for added noise immunity. Fig. 2-12 shows the pin assignments.

An I/O card, such as Pro-Log's 7605 card, along with an RC704 cable can be used to control Segment Select. One output bit or line can control one segment. A segment can be made up of one or more cards.

As shipped, the card is enabled when the Segment Select line is in the high state. The polarity can be reversed by removing jumper W3 from position 1-2 and replacing it with one at position 3-4. See Fig. 2-4.

With jumper W3 in position 1-2 the Segment Select line may be left unconnected. A pull-up resistor provided on the line will hold it in the active condition. If jumper W3 is in position 3-4 however, the line must be controlled in some manner or the card will remain permanently disabled.

SPECIFICATIONS

Figures 2-10 and 2-11 are electrical and environmental specifications. Figures 2-12 and 2-13 describe the specifications for the interface connections and card edge connections.

Figures 2-14 through 2-18 are the timing requirements necessary for the 7702A.

MECHANICAL SPECIFICATIONS

The 7702A meets all general mechanical specifications of the STD BUS.

MNEM.	Recommended Operating Limits				Absolute Non-Operating Limits		
	PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
V_{CC}	Supply Voltage	4.65	5.00	5.35	0	7.00	Volts
—	Free Air Temperature	0	+25	+55	-40	+75	°C
—	Humidity	5		95	5	95	%RH

Figure 2-10. 7702A Electrical and Environmental Specifications.

MNEM.	PARAMETER	MIN	TYP	MAX	UNITS
ICC	VCC Supply Current		425	505	Milliamps*

***NOTE:** Assumes all memory sockets loaded with 2716 EPROMs with one selected and seven in standby. For unused 2716 sockets, subtract 100mA maximum selected or 25mA maximum in standby. Using 2Kx8 static RAMs (OKI MSM 2128) maximum current would be 1.4 A (145 mA per device, max.)

Figure 2-11. 7702A Electrical Characteristics.

PIN NUMBER	INPUT (LSTTL LOADS)		PIN NUMBER	
MNEMONIC				MNEMONIC
SEGMENT[1]	5	2	1	GND

[1] Selectable Logic Polarity

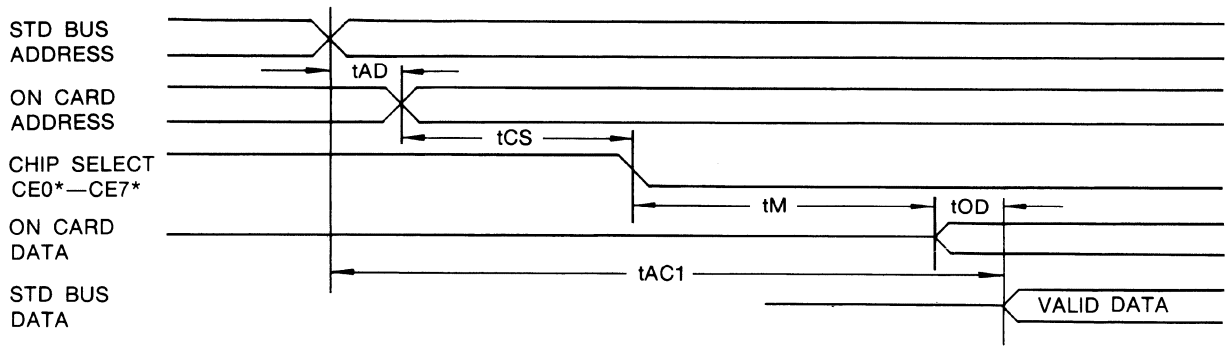
Figure 2-12. 7702A Segment Connector Pin List.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	VCC		+5 VOLTS	1		VCC	+5 VOLTS
4	GND		GROUND	3		GND	GROUND
6			-5V	5			-5V
8	1	55	D7	7	55	1	D3
10	1	55	D6	9	55	1	D2
12	1	55	D5	11	55	1	D1
14	1	55	D4	13	55	1	D0
16	2		A15	15		1	A7
18	2		A14	17		1	A6
20	1		A13	19		1	A5
22	1		A12	21		1	A4
24	1		A11	23		1	A3
26	1		A10	25		1	A2
28	1		A9	27		1	A1
30	1		A8	29		1	A0
32	1		RD*	31		1	WR*
34	1		MEMRQ*	33			IORQ*
36	1		MEMEX	35			IOEXP
38			MCSYNC*	37			REFRESH*
40			STATUS 0*	39			STATUS 1*
42			BUSRQ*	41			BUSAK*
44			INTRQ*	43			INTAK*
46			NMIRQ*	45			WAITRQ*
48			PBRESET*	47			SYSRESET*
50			CNTRL*	49			CLOCK*
52	IN		PC1	51	OUT		PC0
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

* Designates active low-level logic

[1] Selectable logic polarity

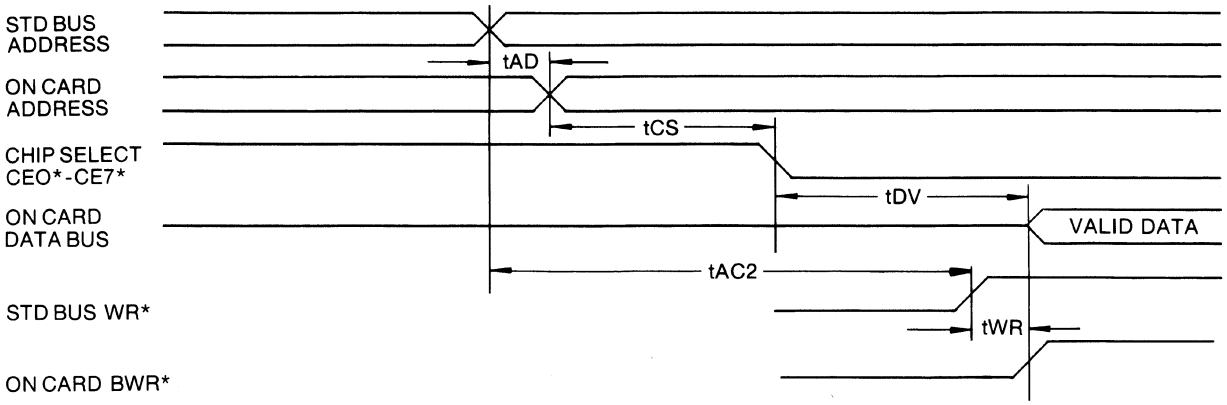
Figure 2-13. 7702A Edge Connector Pin List.



SYMBOL	PARAMETER	NANOSECONDS		
		MIN	TYP	MAX
tAC	Minimum safe access time for read	175	—	—
tAD	Address buffer time delay	—	15	30
tCS	Chip select logic time	—	35	60
tOD	Data bus buffer time delay	—	15	30
tM	Data buffer enable time	—	60	100

All above times are assuming that RD*, MEMRQ*, MEMEX, and SEGMENT SELECT* are active prior to STD BUS address becoming valid.

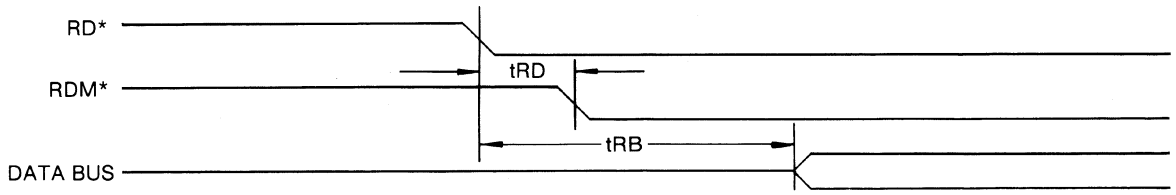
Figure 2-14. 7702A Address Access Time.



SYMBOL	PARAMETER	NANOSECONDS		
		MIN	TYP	MAX
tAC	7702A minimum safe write cycle time	220	—	—
tAD	Address buffer delay time (STD BUS to memory socket)	—	18	30
tCS	Chip select logic time (STD BUS to memory socket)	—	35	60
tDV	Chip select to data valid time (STD BUS to memory socket)	—	60	100
tWR	Write buffer delay (STD BUS to memory socket)	—	12	18

All above times are assuming that WR*, MEMRQ*, MEMEX and SEGMENT are true prior to STD BUS address becoming true.
A memory device with an access time equal to tDV was used here. A memory device faster than tDV will not improve the access time of the card.

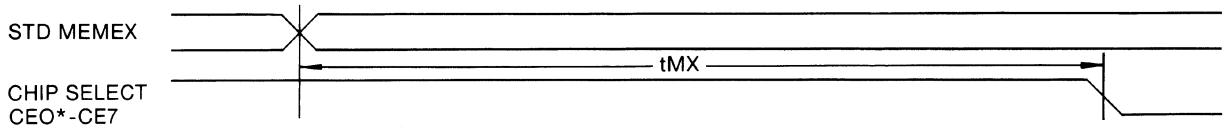
Figure 2-15. 7702A Timing for Write.



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tRD	Time RD* to RDM*	25	50
tRB	Time RD* to data bus buffer enabled	—	100

RD* can go active up to 115 nseconds after MEMRQ* and up to 125 nseconds after address valid without affecting access time. If RD* comes later the time should be added to the minimum access time of the card. Normally RD* goes true during the memory device access time and therefore does not affect addess time for the card.

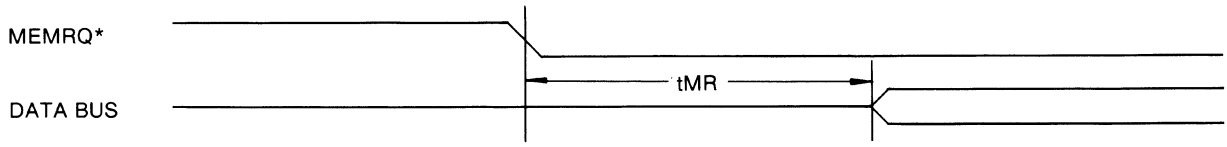
Figure 2-16. 7702A Timing for READ



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tMX	Time MEMEX active to chip select* active	45	75

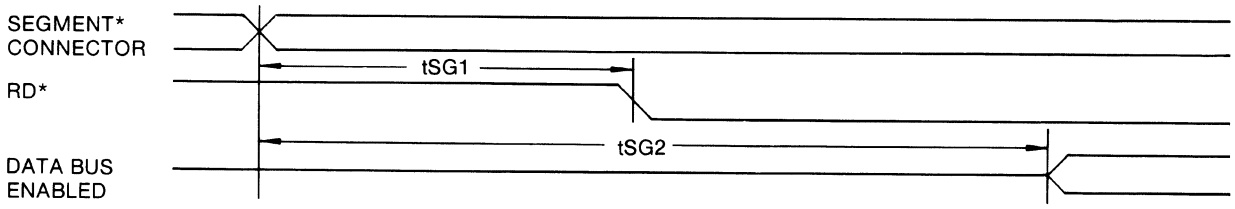
The above parameter is true if all other signals are active prior to MEMEX going active.

Figure 2-17. 7702A MEMEX Timing



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tMR	MEMRQ* active until data bus buffer enabled.	—	92

Figure 2-18. 7702A MEMRQ* Timing.



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tSG1	SEGMENT active to RD*	40	65
tSG2	SEGMENT active to data bus driver enabled	70	120

The above parameters are true if all other signals are active prior to SEGMENT* going active.

Figure 2-19. 7702A SEGMENT Timing.

SECTION 3
Operation and Programming

INTRODUCTION

This section describes the function and use of the 7702A card. The card is designed to be a versatile part of your memory system.

It can be used in both small and large-scale applications. By using the MEMEX and Segment Select lines described in this section, the 7702A can fill the memory requirements of virtually any system.

MEMEX

The MEMEX line is part of the STD BUS. It is used as a memory bank select line. Using this line allows two banks of memory to occupy the same address field. Only one of the banks is selected at a time, depending on the logic state of the MEMEX line.

It is normally controlled by a memory segment controller or an output port. The segment controller or output port can be either on the processor card or on some other card in the system. Some Pro-Log processor cards have an onboard output port for controlling MEMEX.

MEMEX Example

An example of how MEMEX can be used is shown in Figure 3-1. It shows a five 7702A memory cards and a 7804 Processor Card with no onboard memory. Three of the 7702A cards are permanently enabled. That is, they ignore MEMEX. These three 7702A cards contain RAM from address 4000 to FFFF. Of the remaining two cards, only one is enabled at a time depending on whether the MEMEX line is high or low.

At power-up, the MEMEX port is low. The primary memory bank is therefore enabled. The processor can thereafter choose which bank it will work with just by manipulating the MEMEX line.

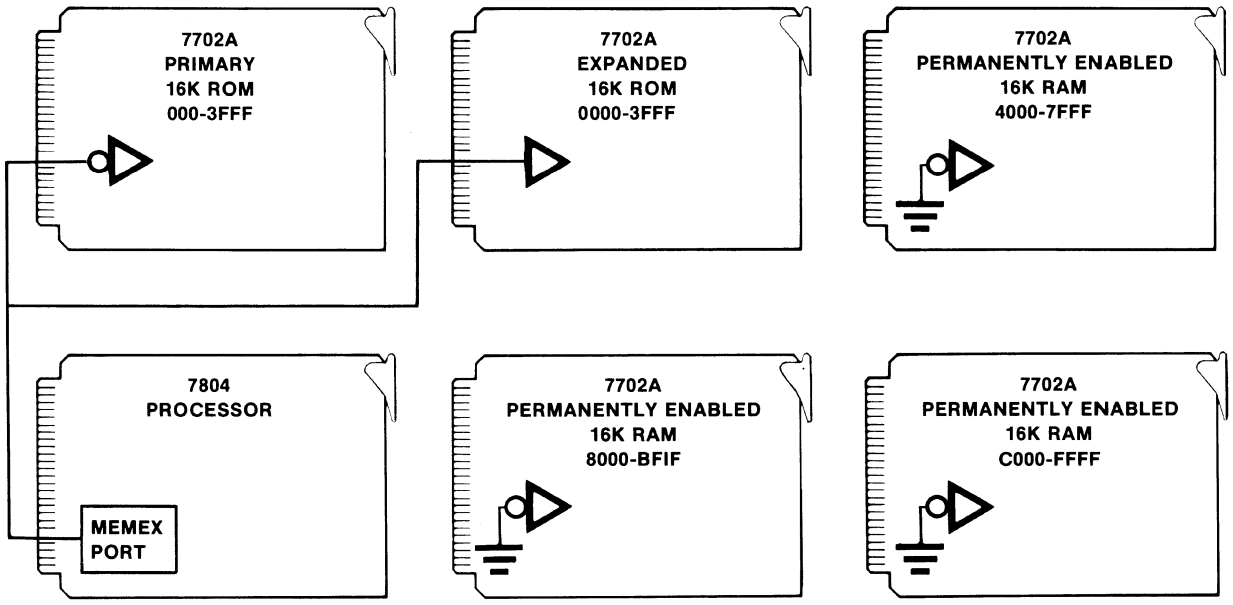


Figure 3-1. 7702A MEMEX Example.

SEGMENT SELECT

The Segment Select line is not a part of the STD BUS, but is an external line which must be connected on the card ejector side of the 7702A, when it is used. Figure 2-2 shows the location of the connector. The purpose of the line is to allow the 7702A card to participate in large scale memory bank select schemes, where multiple cards occupy the same address field.

Whereas the MEMEX line can be used to select one of two banks of memory, the segment Select line can choose one of any number of memory banks.

The line is normally controlled by a memory segment controller or by output ports. An I/O card such as Pro-Log's 7605 card along with an RC704 cable can be used to control the line. One output port can control eight banks of memory.

Figure 3-2 is an example of how the line can be used. It shows a memory system with three 7702A's mapped to the same address range. The 4K RAM is on the processor card and is permanently enabled. The ROM is on three cards. Each card has its Segment Select line connected to a bit of an output port on an I/O card.

At power up, the output port bits would be low. One of the 7702A cards would be configured for low-level active Segment Select. The other two would be high level active. Therefore, one of the cards would automatically be selected at power up. The processor could thereafter choose which card it wanted simply by writing to the output port.

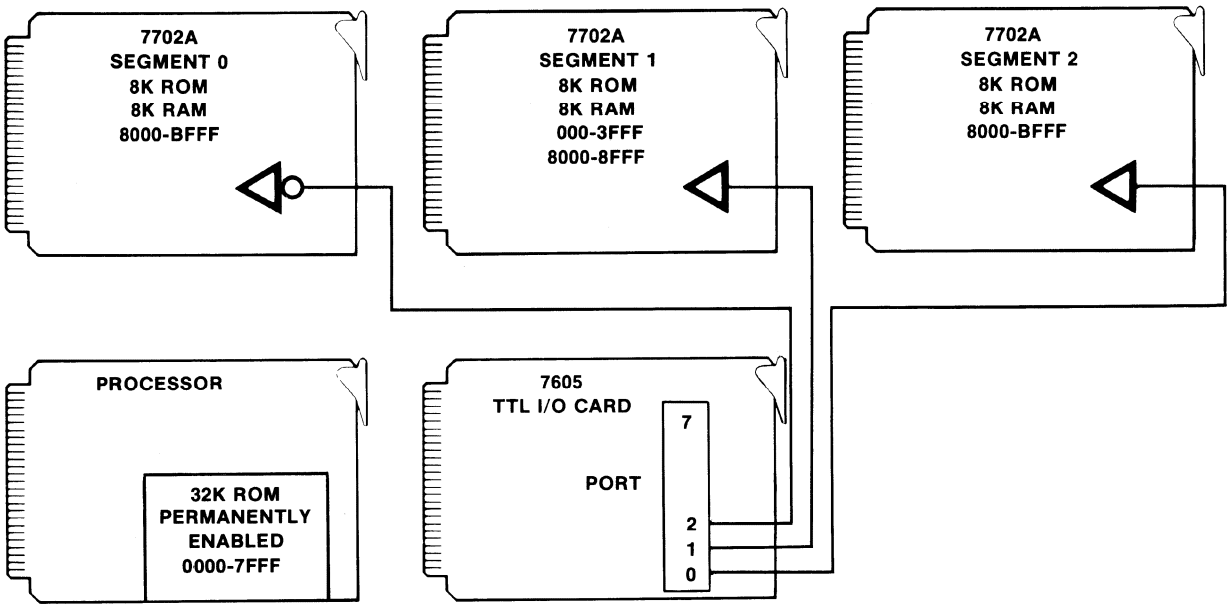


Figure 3-2. 7702A Segment Select Example One.

SECTION 4
Operating Software

Section Four is usually reserved for operating software for STD Series 7000 cards. The 7702A requires no special software.

SECTION 5
Maintenance

INTRODUCTION

This section contains an overview of the 7702A's circuitry, return for repair procedures, and the two-year limited warranty. The schematic and assembly drawing are located at the back of this manual.

OPERATIONAL OVERVIEW

Address Buffers

Address lines A0-A10 connect to all eight memory sockets and are buffered to reduce data bus noise and loading (see Figure 5-1).

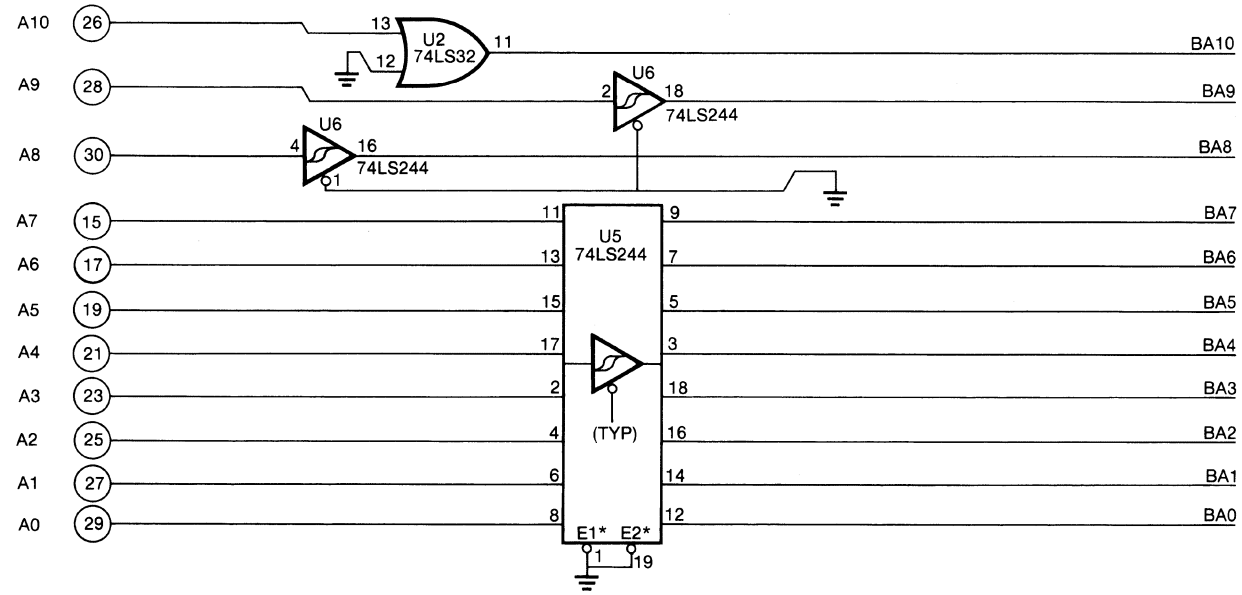


Figure 5-1. 7702A Address Buffers.

Address Decoder

The 7702A's eight memory sockets are selected via IC's U1 and U7. Using jumpers W1, W2, and inverter U1 the upper address lines are fed to U7, the Chip Select Decoder. The MEMEX line is also fed into U7. The level of MEMEX that will enable your card is determined at U1 and W4. Jumpers W5 are used to disable individual sockets (see Figure 5-2).

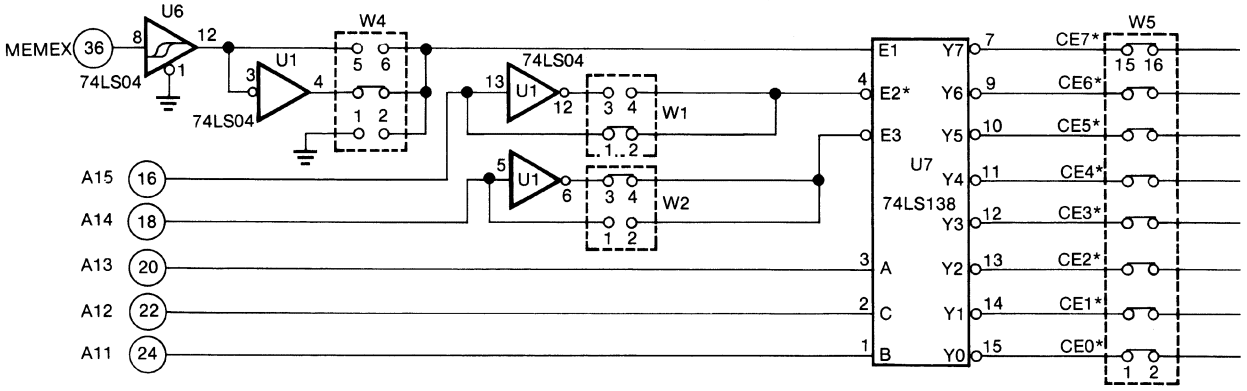


Figure 5-2. 7702A Address Decoder.

Read and Write Buffers

RD* and WR* signals are buffered and connect to multiple chips on the 7702A. Also the RD* and WR* buffer will only be enabled if the MEMRQ* and Segment Select signals are active. Otherwise the outputs BWR* and BRD* will be pulled high via resistors R8 and R7 (see Figure 5-3).

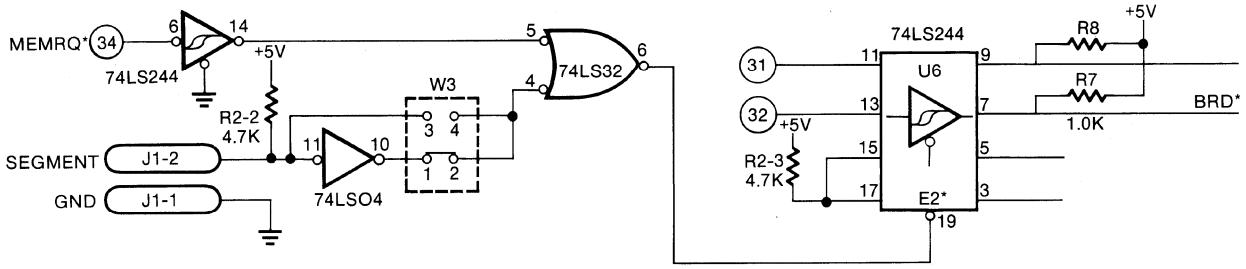


Figure 5-3. 7702A READ and WRITE Buffers.

Data Bus Buffer

The bidirectional data bus buffer U4 is enabled whenever MEMRQ*, SEGMENT SELECT are active, and a chip is selected. The direction of the buffer is controlled by the buffered Read signal BRD* (see Figure 5-4).

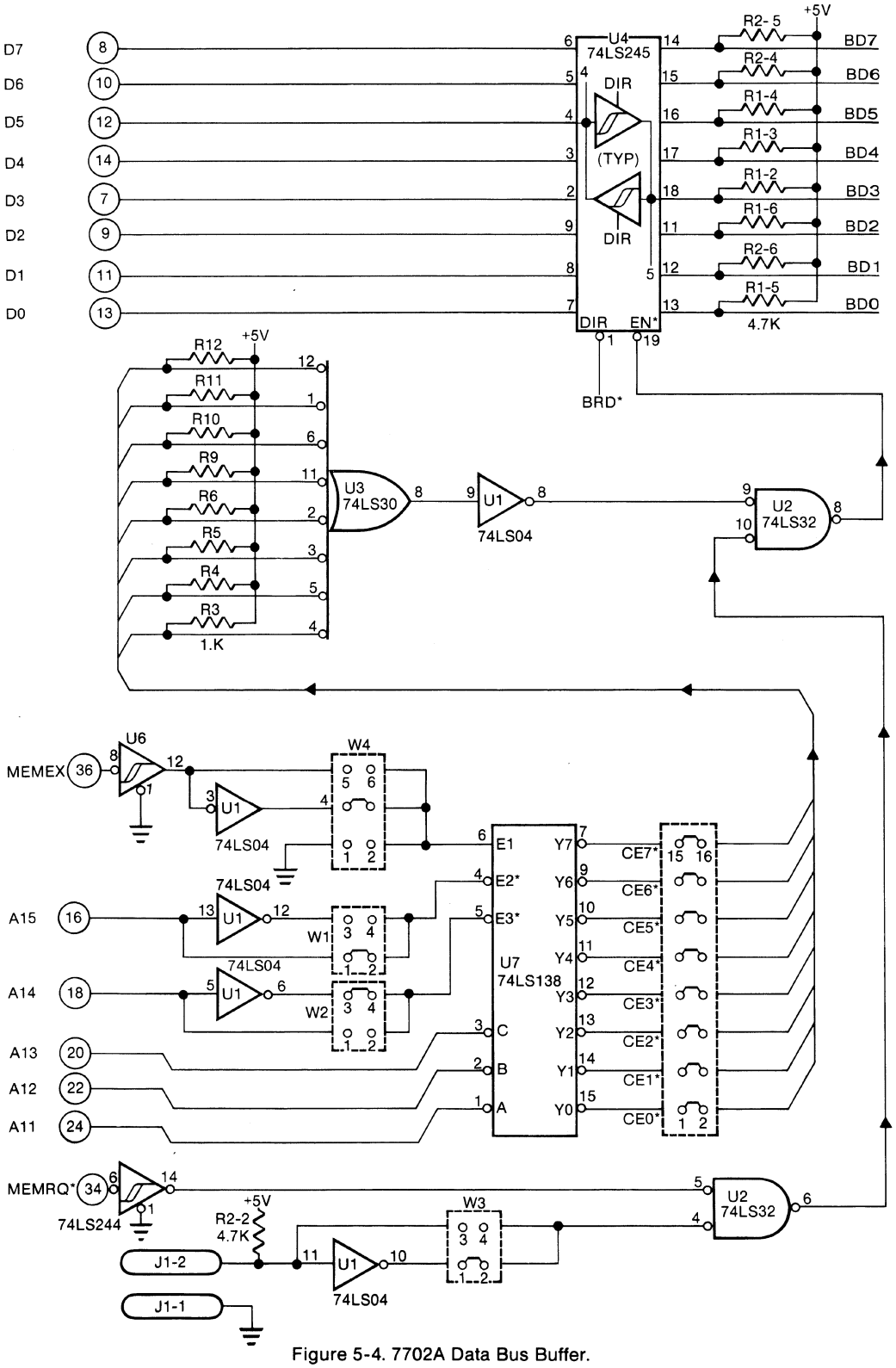


Figure 5-4. 7702A Data Bus Buffer.

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call our factory direct at (408) 372-4593, and ask for CUSTOMER SERVICE.
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, reason for return, and the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Package the equipment in a solid cardboard box secured with packing material.

   CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.
5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, Calif. 93940

   Reference CRO #_____

International Customers:

Equipment repair is handled by your local Pro Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

Appendix A
Documentation

REFERENCE DRAWINGS

The schematic (Figure D-1) and assembly drawing (Figure D-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. They may differ in some respects from the card and documentation that the user receives from Pro-Log.

The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.

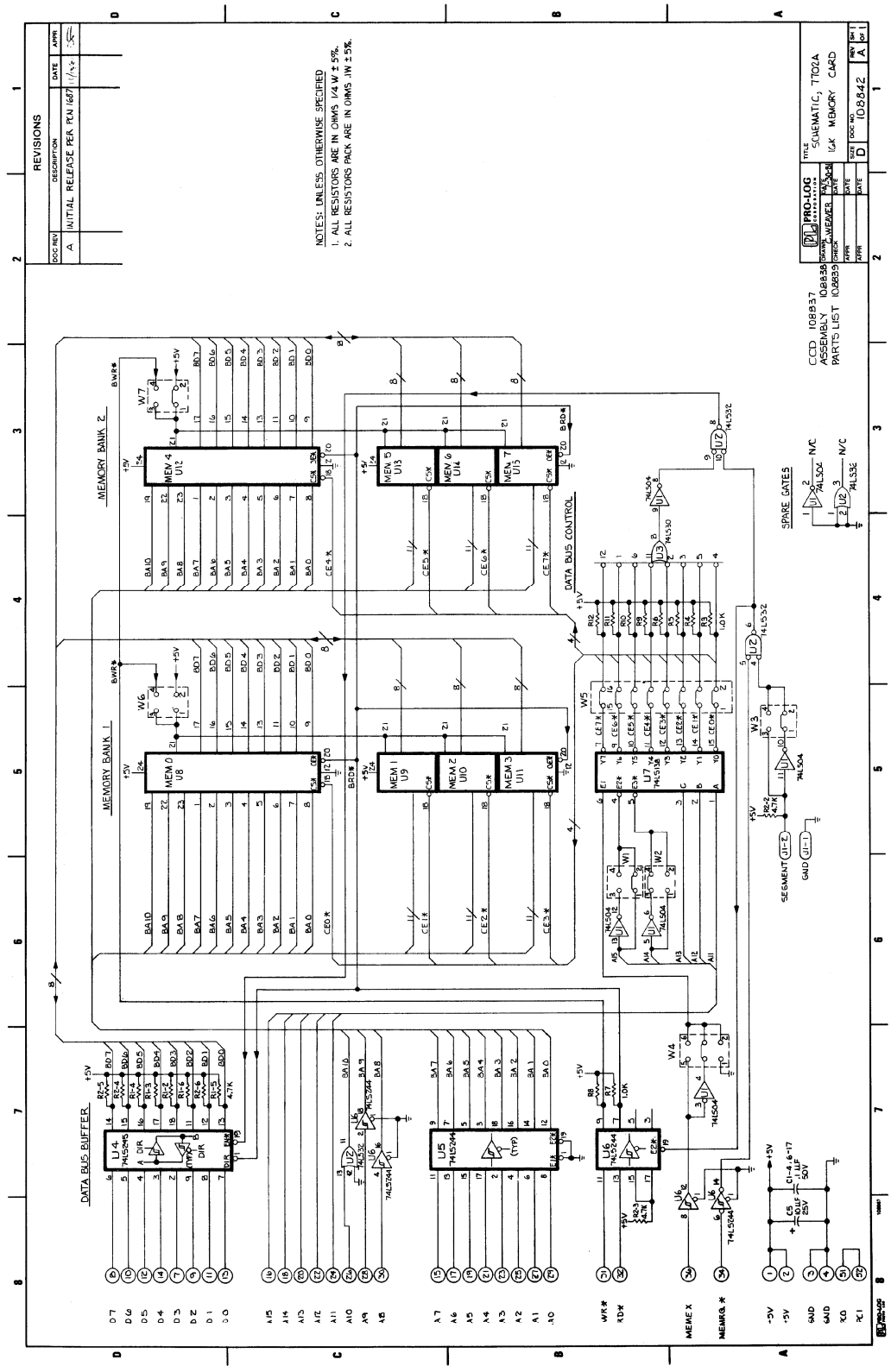


Figure A-1. 7702 A Schematic.

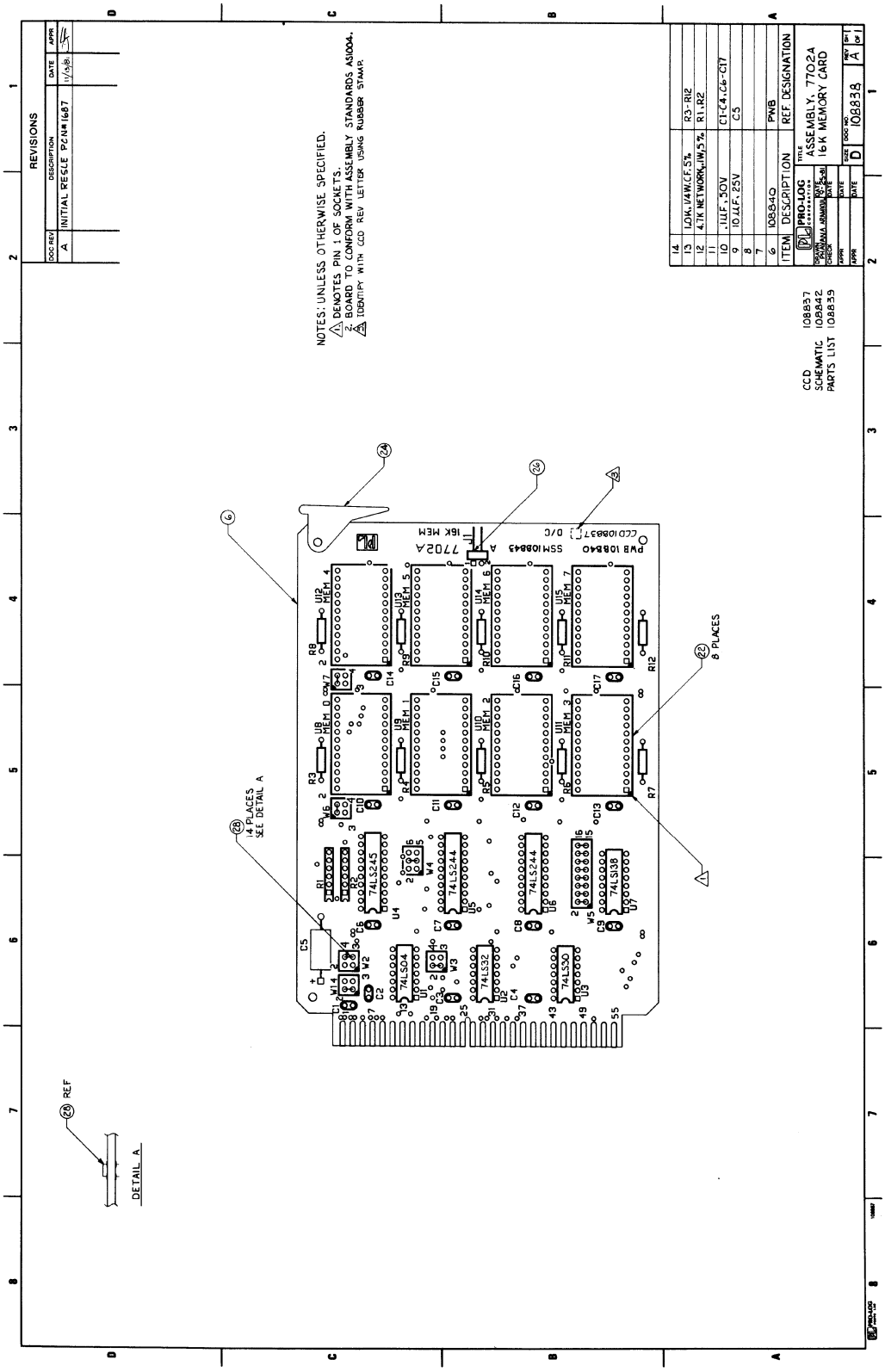


Figure A-2. 7702 A Assembly.